
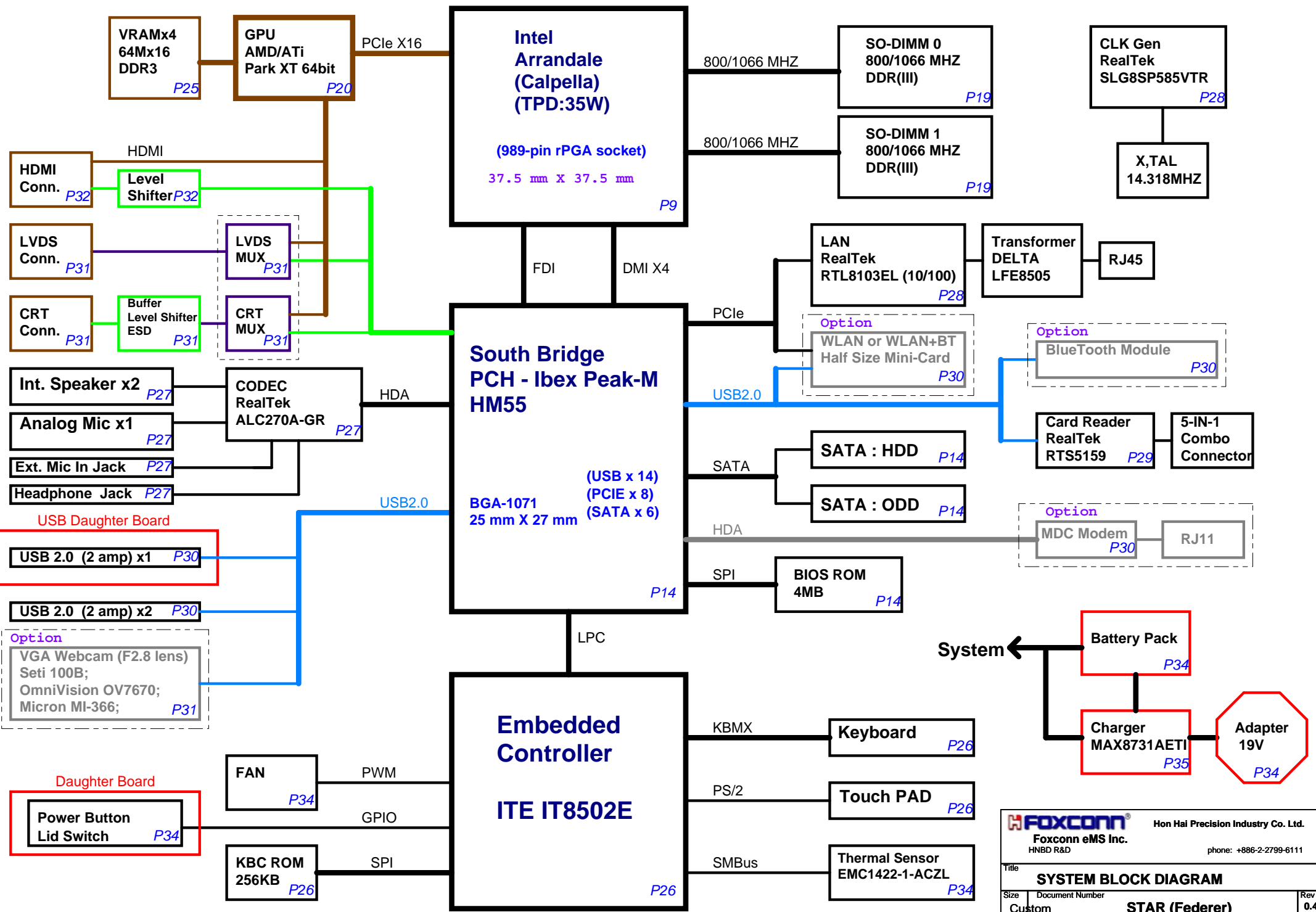
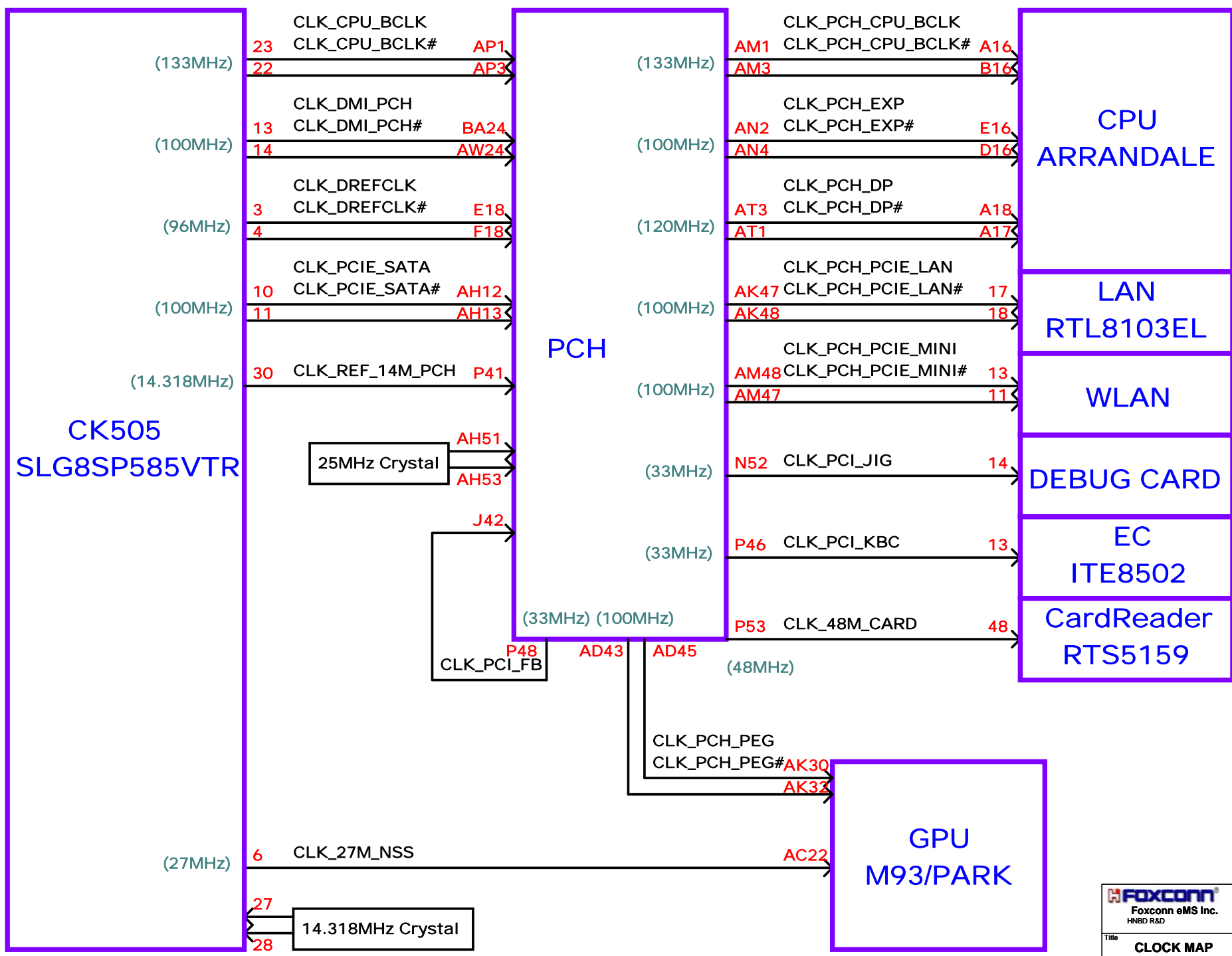


| | | | | | |
|----|----|--------------------------|----|----|---------------------------|
| 01 | -- | COVER SHEET | 21 | -- | VGA_S3 (IO) 2/5 |
| 02 | -- | SYSTEM BLOCK DIAGRAM | 22 | -- | VGA_S3 (DDR3) 3/5 |
| 03 | -- | CLOCK MAP | 23 | -- | VGA_S3 (DP) 4/5 |
| 04 | -- | POWER MAP | 24 | -- | VGA_S3 (POWER) 5/5 |
| 05 | -- | POWER SEQUENCY DIAGRAM | 25 | -- | VRAM (DDR3) |
| 06 | -- | POWER SEQUENCY TIMING | 26 | -- | EC+KBC (IT8502E) |
| 07 | -- | SMBUS MAP | 27 | -- | CODEC/JACK/SPEAKER/MIC |
| 08 | -- | RESET SIGNAL MAP | 28 | -- | LAN (RTL8103EL)/CLOCK GEN |
| 09 | -- | Calpella (DMI,PEG,FDI) | 29 | -- | Card Reader |
| 10 | -- | Calpella (CLK,MISC,JTAG) | 30 | -- | WLAN/BT/MDC/USB/MOUNTING |
| 11 | -- | Calpella (DDR3) | 31 | -- | LVDS/CRT/Webcam |
| 12 | -- | Calpella (POWER/GND) | 32 | -- | HDMI |
| 13 | -- | Calpella (GRAPHIC POWER) | 33 | -- | DCIN/Battery/OCP/FAN |
| 14 | -- | PCH (HDA,JTAG,SATA) | 34 | -- | PWR_Charger MAX8731AETI |
| 15 | -- | PCH (PCI-E,SMBUS,CLK) | 35 | -- | 5V/3.3V SN0608098RHB |
| 16 | -- | PCH (DMI,FDI,GPIO,LVDS) | 36 | -- | Vcore MAX17030 |
| 17 | -- | PCH (PCI,USB,NVRAM,GPIO) | 37 | -- | 1.1V VTT/+V1.05RUN |
| 18 | -- | PCH (POWER) | 38 | -- | 1.5VDDR3+0.75V+V1.8RUN |
| 19 | -- | DDR3(SO-DIMM_0&1) | 39 | -- | PWR_Others power plane |
| 20 | -- | VGA (PCI-E/STRAP) 1/5 | 40 | -- | CPU VREG & Decoupling |
| | | | 41 | -- | ATVDD/+VPCIE |

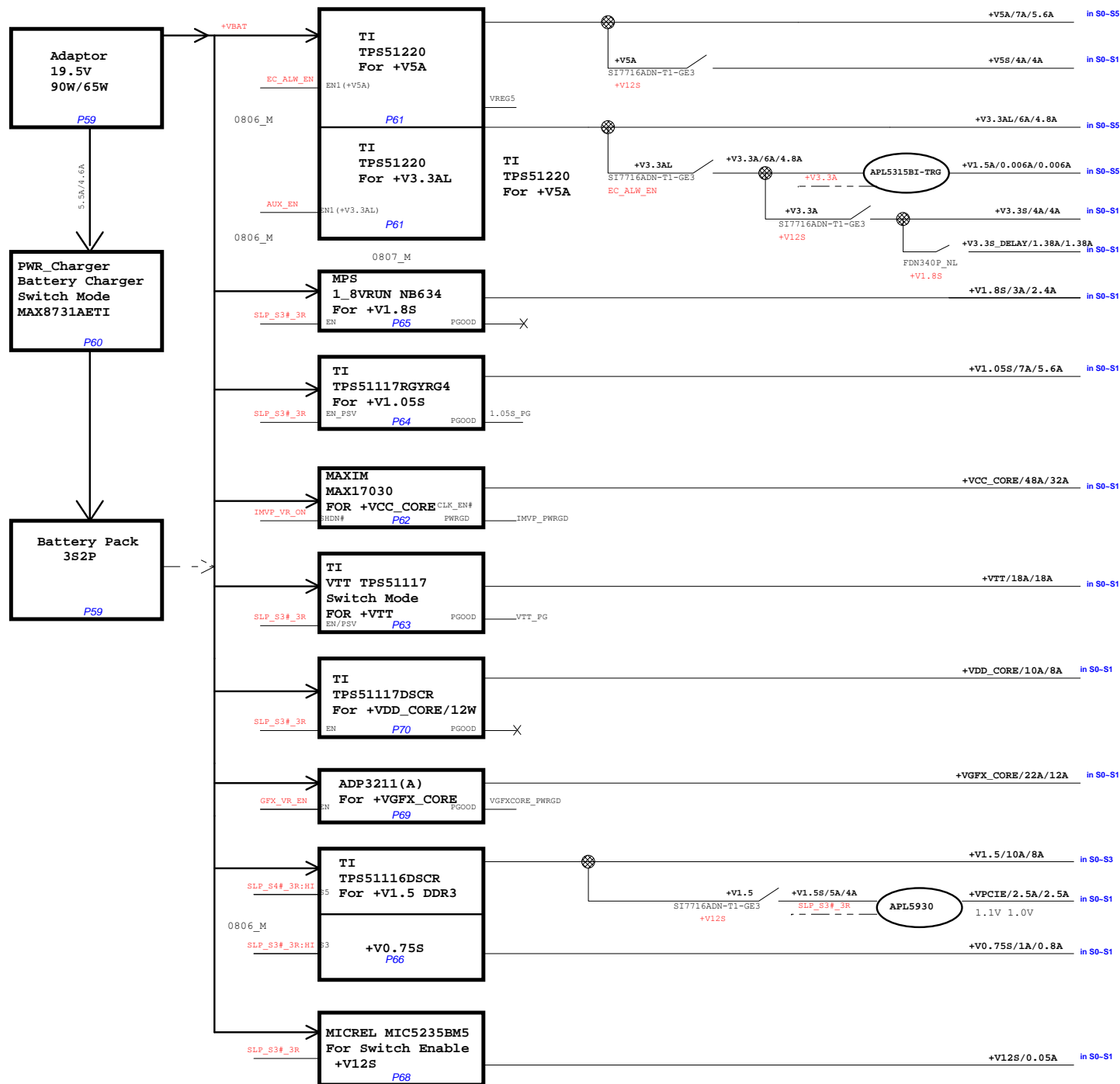
| | | |
|-----------|----------|-----------|
| P. Leader | Check by | Design by |
| | | |

| | | |
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|  Foxconn EMS Inc. HNBD R&D | | Hon Hai Precision Industry Co. Ltd. phone: +886-2-2799-6111 |
| Title | | |
| Index Page | | |
| Size | Document Number | Rev |
| Custom | STAR (Federer) | 0.4 |
| Page Modified: Tuesday, December 29, 2009 13:50:37 (UTC/GMT) | | Sheet 1 of 41 |

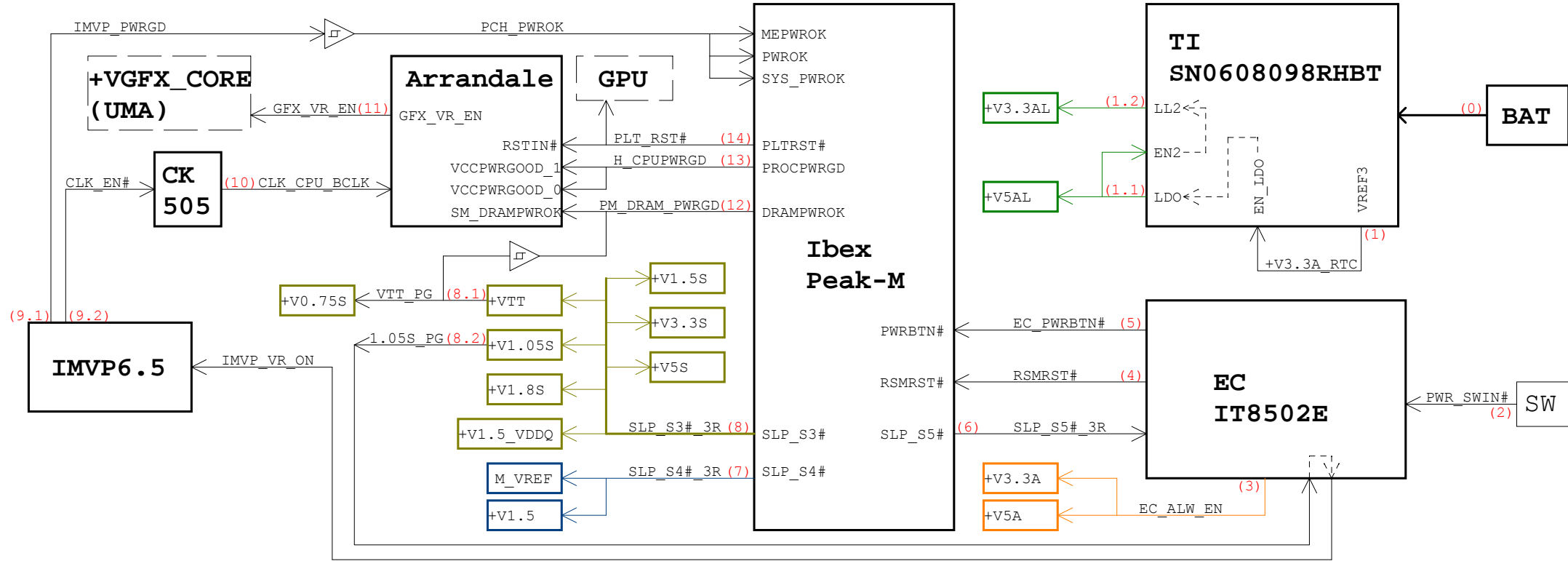




ADAPT_OC_IINP to IT8520
ACIN_EC to IT8520



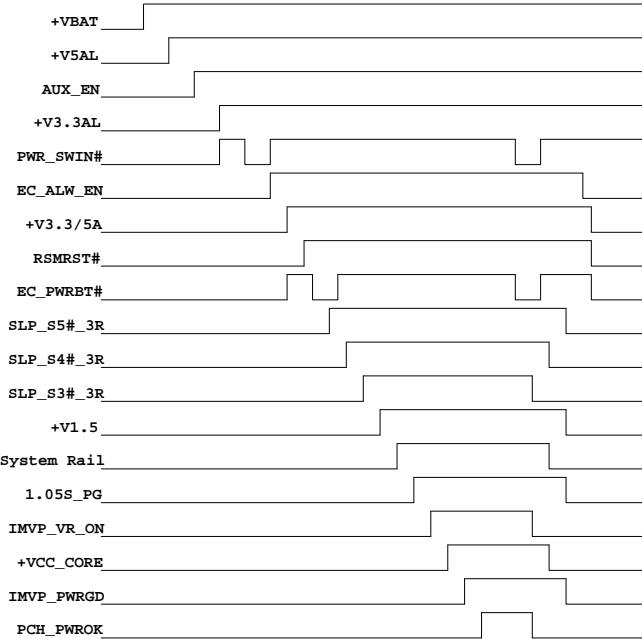
POWER SEQUENCY DIAGRAM



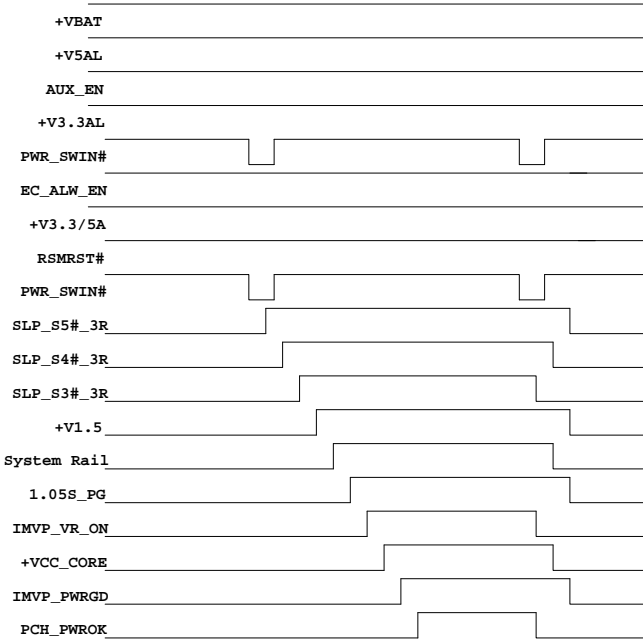
| | Source Rail | EN | PG | Power Status | | | | Remark |
|--------------|-------------|-------------|------------|--------------|----|----------|----------|--------|
| | | | | S0 | S3 | AC S4/S5 | DC S4/S5 | |
| +VBAT | | | | V | V | V | V | |
| +V5AL | +VBAT | +V3.3A_RTC | | V | V | V | V | |
| +V3.3AL | +VBAT | +V5AL | | V | V | V | V | |
| +V5A | +VBAT | EC_ALW_EN | | V | V | V | | |
| +V3.3A | +V3.3AL | EC_ALW_EN | | V | V | V | | |
| +V1.5 | +VBAT | SLP_S4#_3R | | V | V | | | |
| +V0.75S | +V1.5 | VTT_PG | | V | | | | |
| +V1.5S | +V1.5 | RUN_ON_LOAD | | V | | | | |
| +V1.5_VDDQ | +V1.5 | RUN_ON_LOAD | | V | | | | |
| +VCC_CORE | +VBAT | IMVP_VR_ON | IMVP_PWRGD | V | | | | |
| +VTT | +VBAT | SLP_S3#_3R | VTT_PG | V | | | | |
| +VGFX_CORE | +VBAT | GFX_VR_EN | | V | | | | |
| +V1.8S | +VBAT | SLP_S3#_3R | | V | | | | |
| +V1.05S | +VBAT | SLP_S3#_3R | 1.05S_PG | V | | | | |
| +V5S | +V5A | RUN_ON_LOAD | | V | | | | |
| +V3.3S | +V3.3A | RUN_ON_LOAD | | V | | | | |
| +VDD_CORE | +VBAT | SLP_S3#_3R | | V | | | | |
| +V3.3S_Delay | +V3.3S | +V1.8S | | V | | | | |
| +VPCIE | +V1.5S | SLP_S3#_3R | | V | | | | |

POWER SEQUENCE TIMING

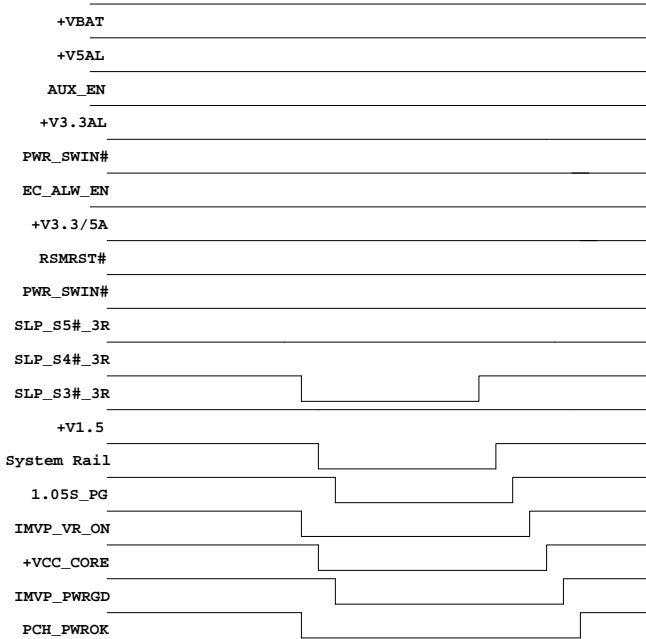
G3(OFF)->S0->S5



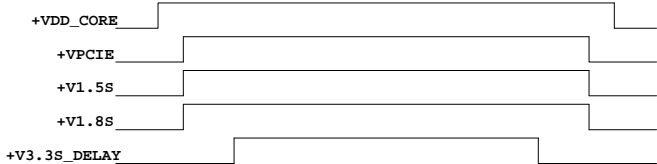
S5->S0->S5



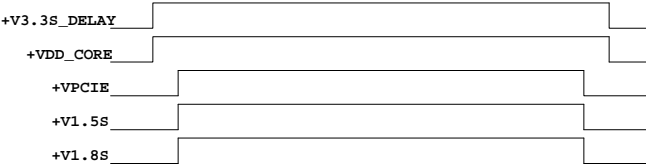
S0->S3->S0



M93 Sequence



Park Sequence



SMBUS&I2C MAP

Discrete
GPU

GPU
M93/Park
S3 Package

PCH

EC
ITE8502

DIMM0

DIMM1

CLOCK
GEN


WLAN

Temp
Sensor

Charger

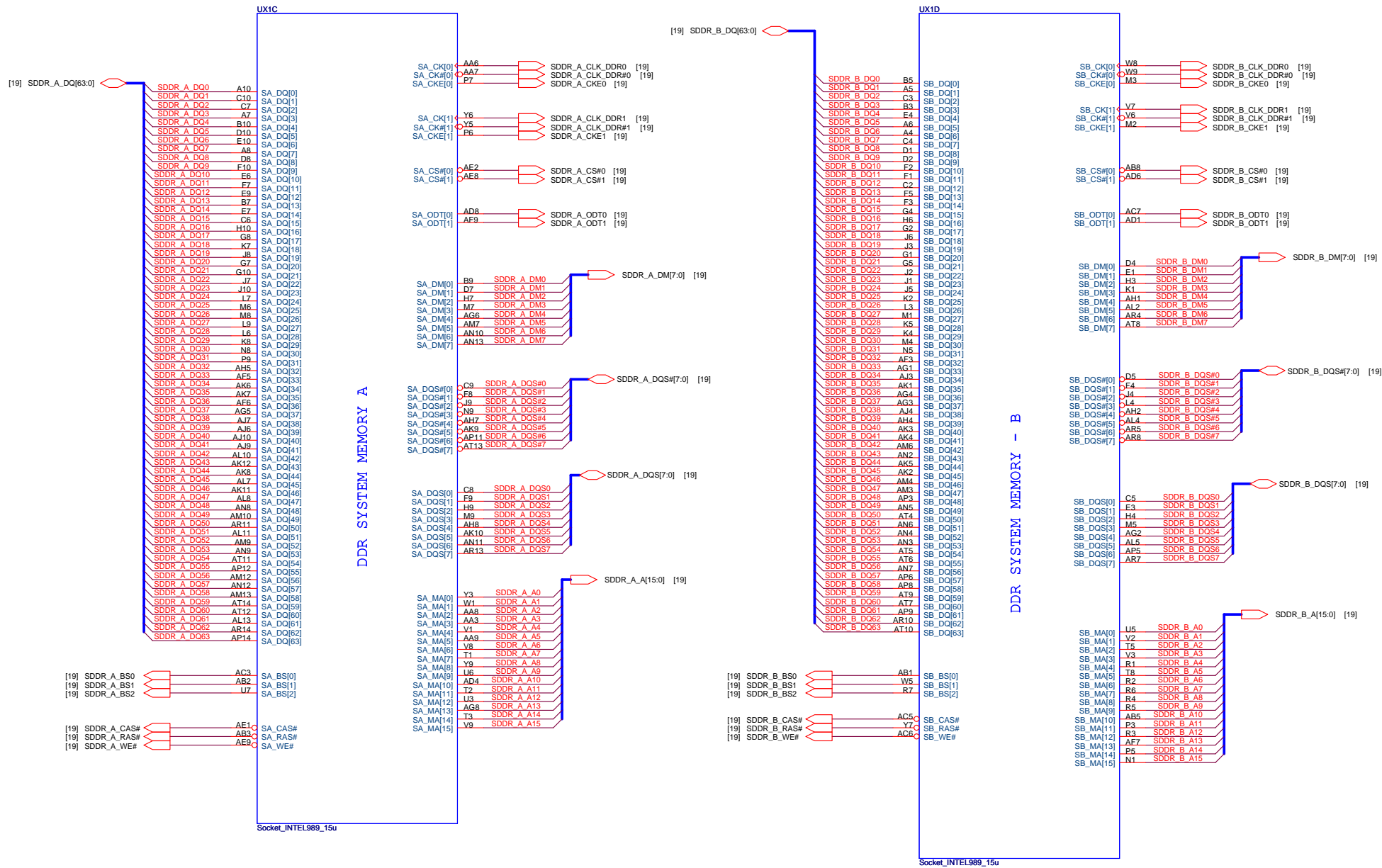
Battery

RESET SIGNAL MAP

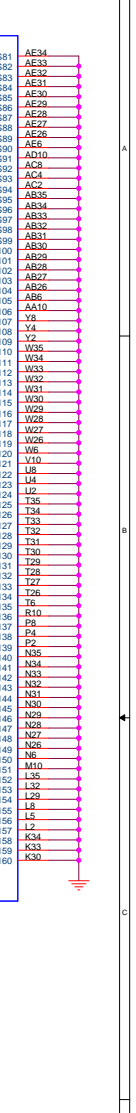
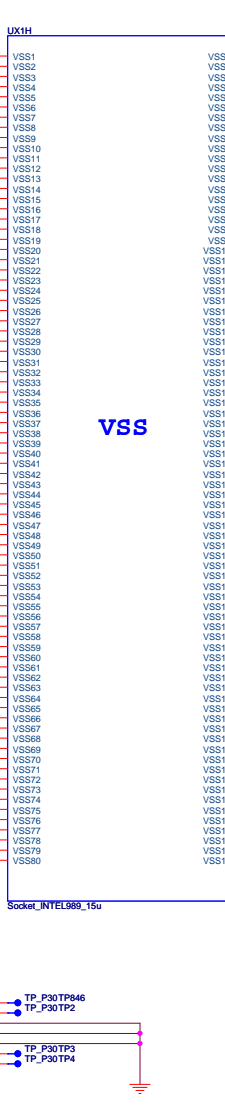
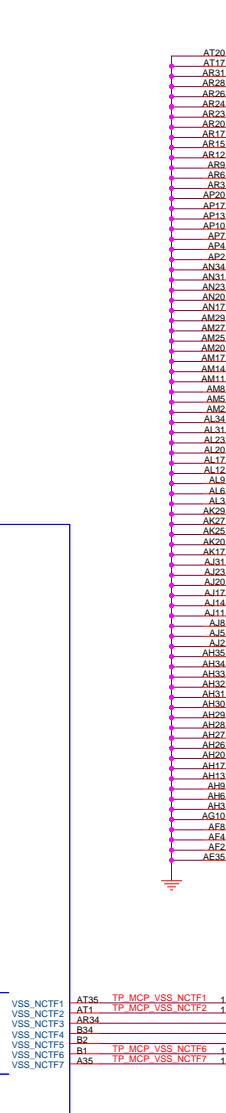
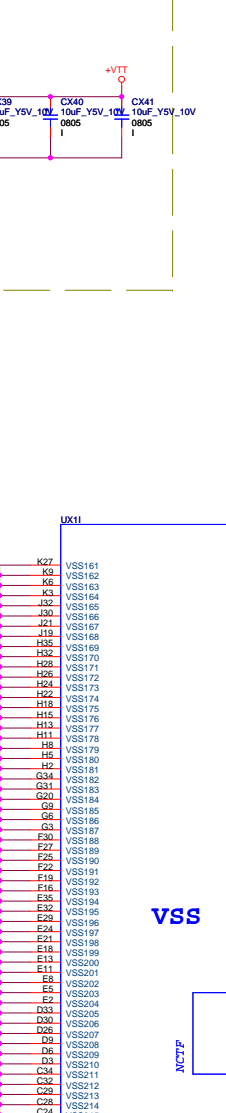
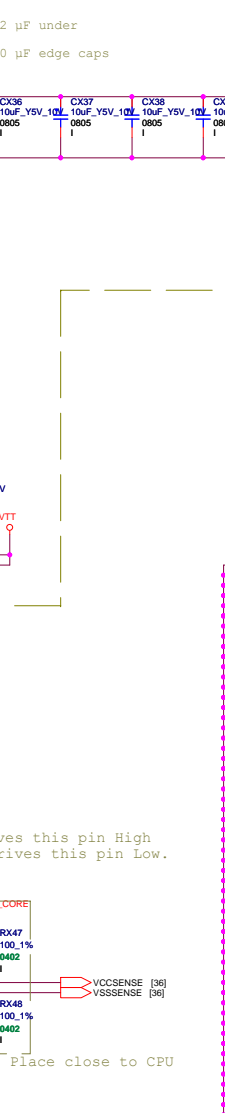
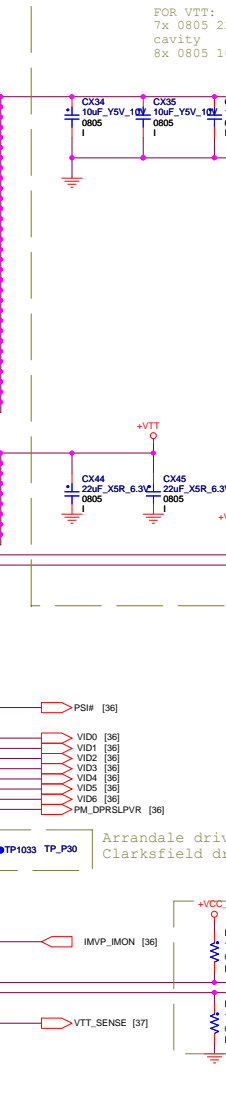
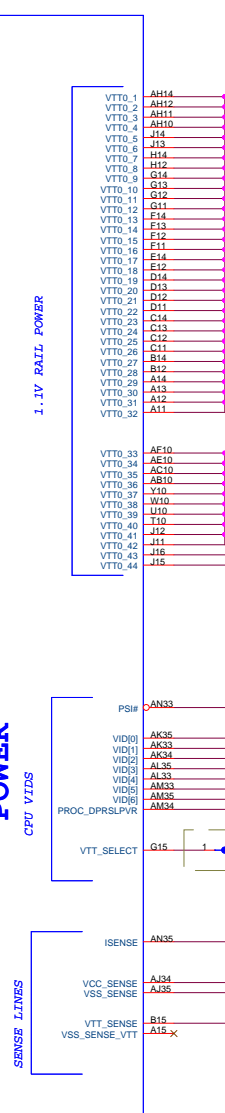
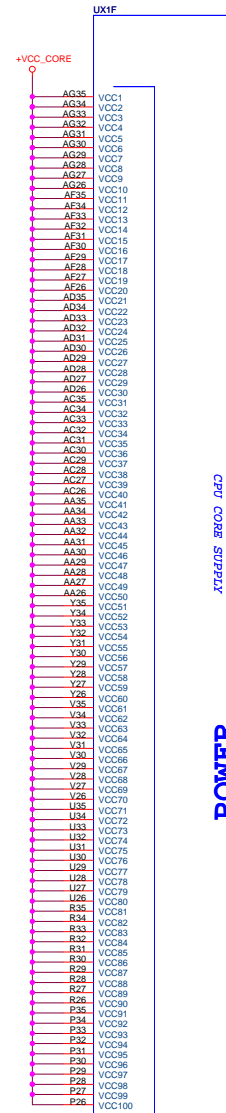
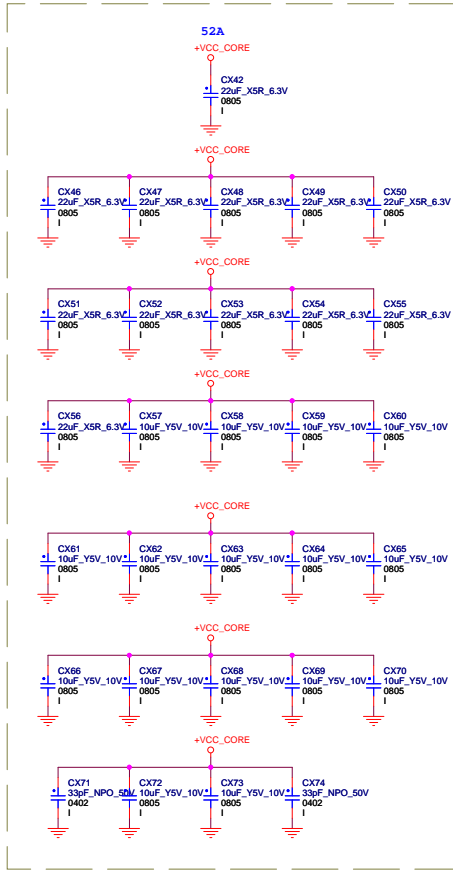
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| Foxconn eMS Inc. | | HNBD R&D | |
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| RESET SIGNAL MAP | | | |
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Place close to chip





FOR VCC:
12x 0805 22 μ F inside cavity,
7x 0805 10 μ F under cavity and 9 x 0805 10
 μ F
between inductor and socket on top layer



+VTT to +VTT [10,13,17,18,26,36,37,40]
+VCC_CORE to +VCC_CORE [36]

FOR VTT:
7x 0805 22 μ F under
cavity
8x 0805 10 μ F edge caps

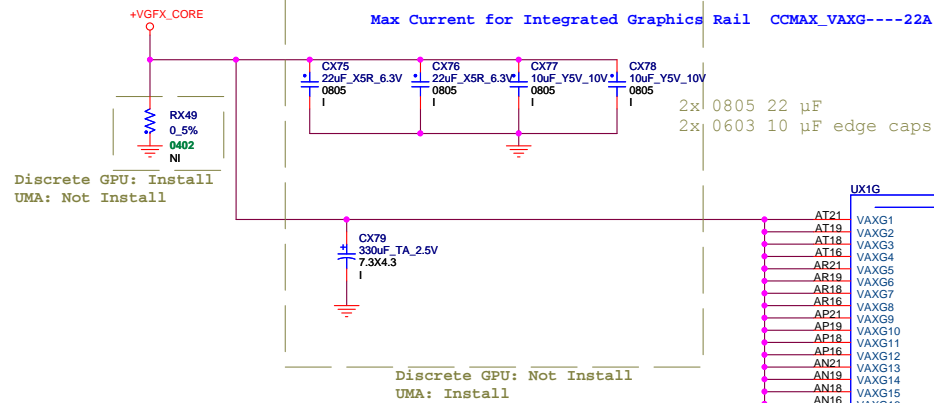
Arrandale drives this pin High
Clarkfield drives this pin Low.

Place close to CPU

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| | | | |
|---|-----------------|----------------------|-----|
| Title | | Calpella (POWER/GND) | |
| Size | Document Number | Rev | 0.4 |
| Custom | STAR (Federer) | | |
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UX1G

AT21 VAXG1
AT19 VAXG2
AT18 VAXG3
AT16 VAXG4
AR21 VAXG5
AR19 VAXG6
AR18 VAXG7
AR16 VAXG8
AP21 VAXG9
AP19 VAXG10
AP18 VAXG11
AP16 VAXG12
AN21 VAXG13
AN19 VAXG14
AN18 VAXG15
AN16 VAXG16
AM21 VAXG17
AM19 VAXG18
AM18 VAXG19
AM16 VAXG20
AL21 VAXG21
AL19 VAXG22
AL18 VAXG23
AK21 VAXG24
AK19 VAXG25
AK18 VAXG26
AK16 VAXG27
AJ21 VAXG28
AJ19 VAXG29
AJ18 VAXG30
AJ16 VAXG31
AH21 VAXG32
AH19 VAXG33
AH18 VAXG34
AH16 VAXG35
AH16 VAXG36

GRAPHICS

POWER

SENSE LINES

GRAPHICS VIDS

DDR3 - 1.5V RAILS

1.1V

1.8V

FDI

PBG & DMT

Socket_INTEL989_15u

+VTTQ [10,12,17,18,28,36,37,40]
+VGFX_COREQ [40]
+V1.5_VDDQ [10,18,28,30,39]
+V1.8SQ [18,38,39]

Discrete GPU: Not Install
UMA: Install

AR22 RX50 0.5% 0402
AT22 RX51 0.5% 0402

GFX_VCC_SENSE [40]
GFX_VSS_SENSE [40]

AM22 GFX_VID0 [40]
AP22 GFX_VID1 [40]
AN22 GFX_VID2 [40]
AP23 GFX_VID3 [40]
AM23 GFX_VID4 [40]
AP24 GFX_VID5 [40]
AN24 GFX_VID6 [40]

AR25 GFX_VR_EN [40]
AT25 GFX_DPRSLPVR [40]
AM24 GFX_IMON [40]

Discrete GPU: Not Install
UMA: Install

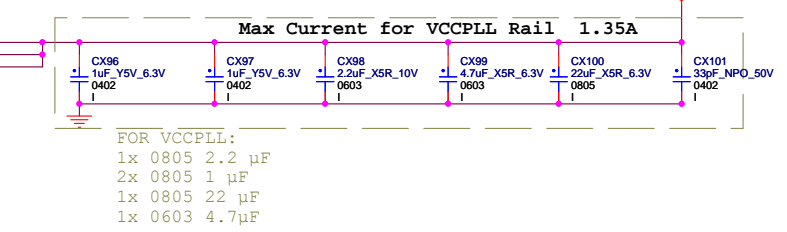
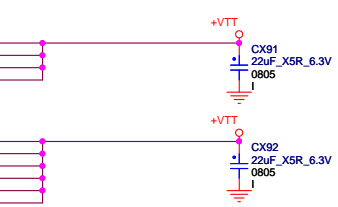
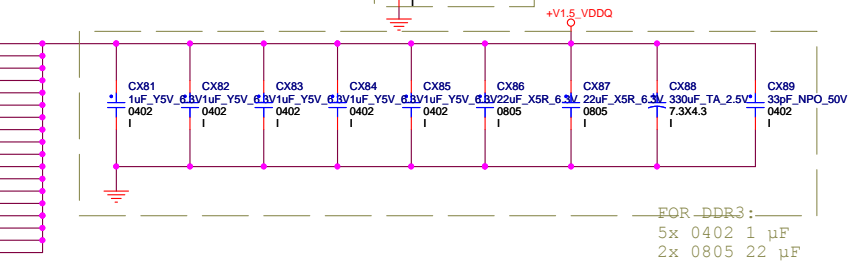
RX63 4.7K_5% 0402

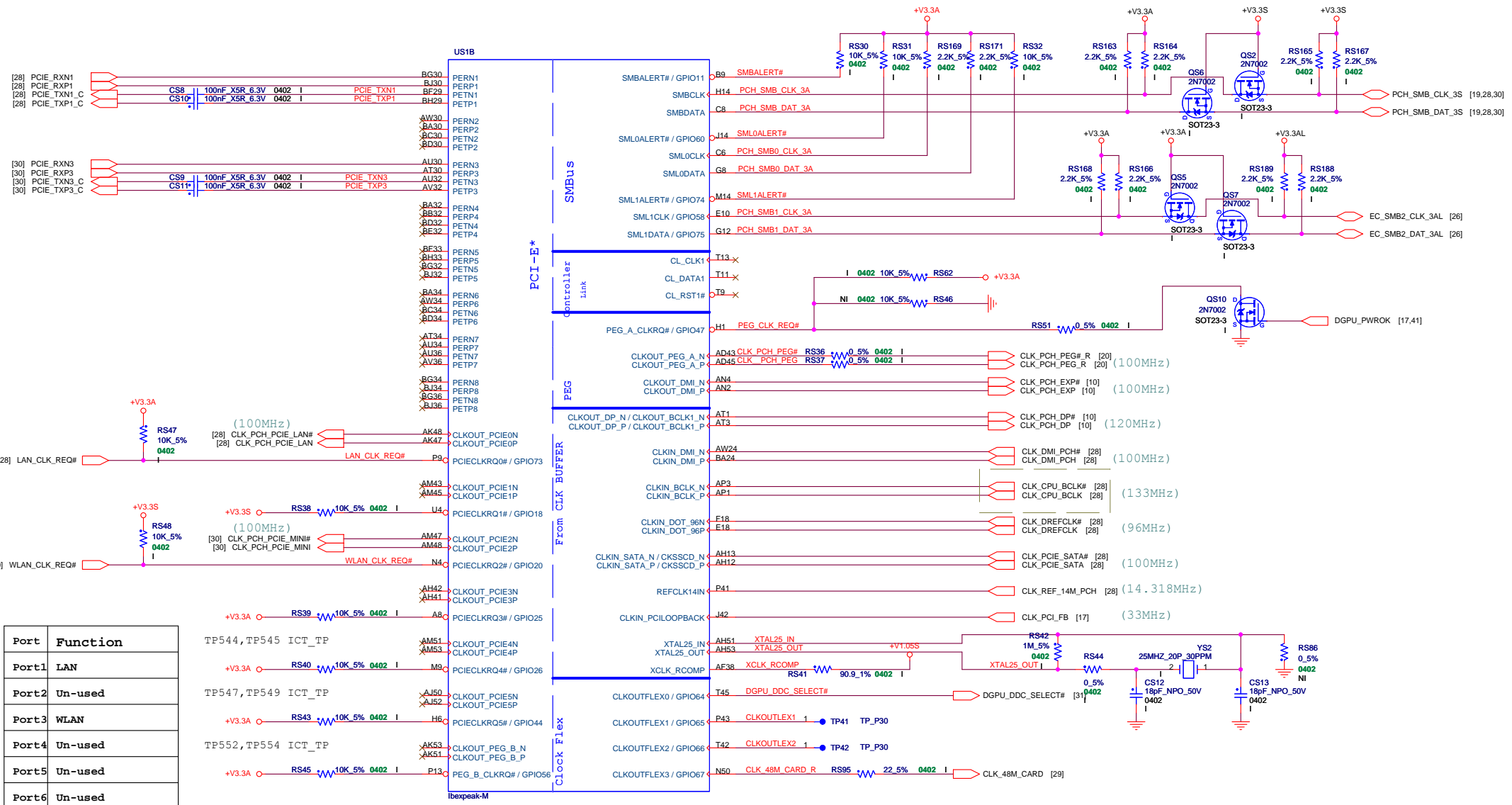
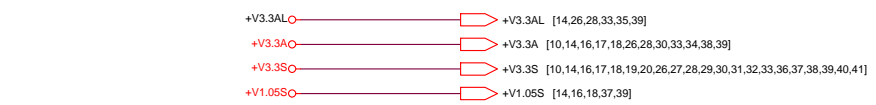
GFX_VR_EN [40]

Discrete GPU: Install
UMA: Not Install

RX52 1K_5% 0402

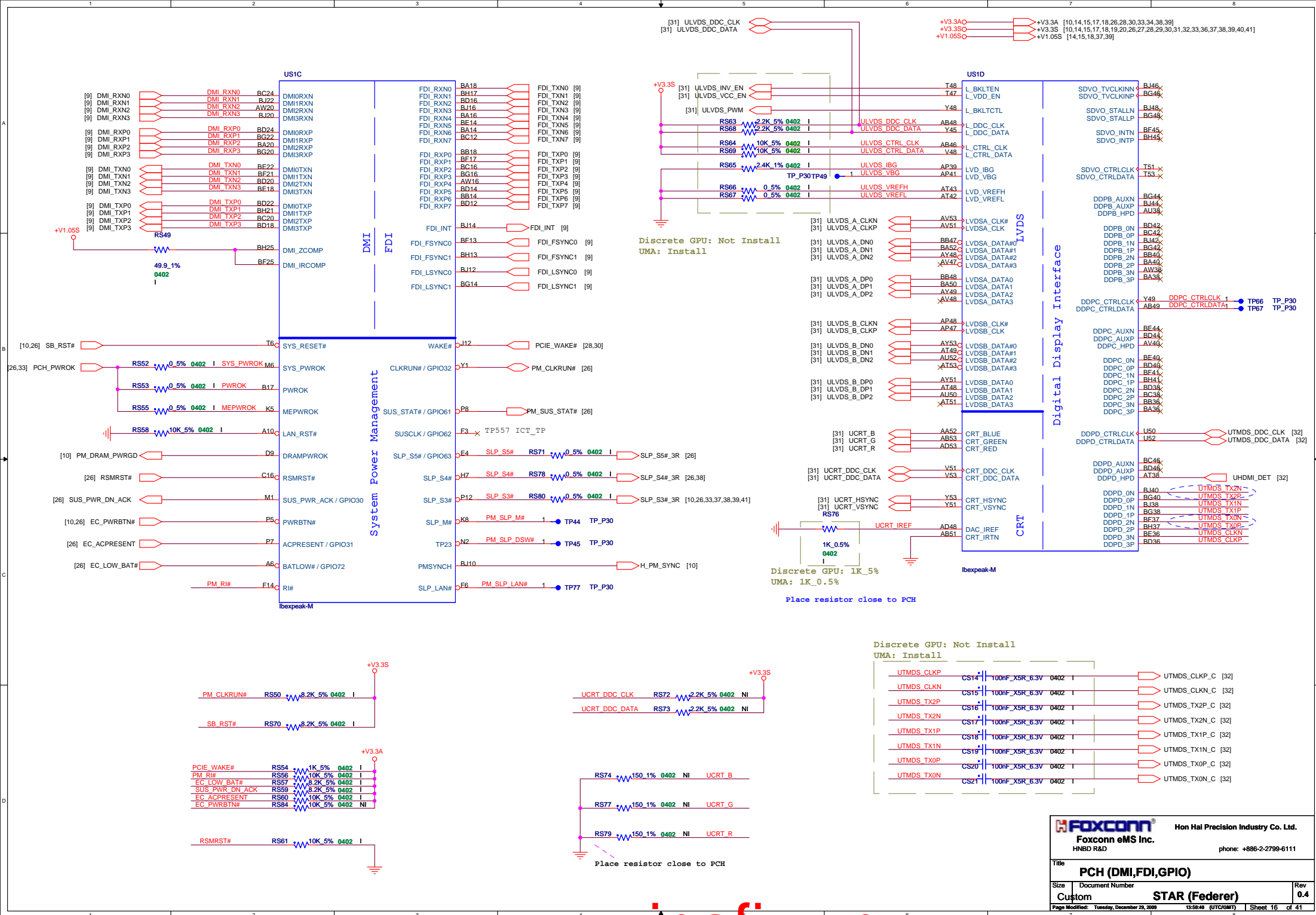
GFX_IMON

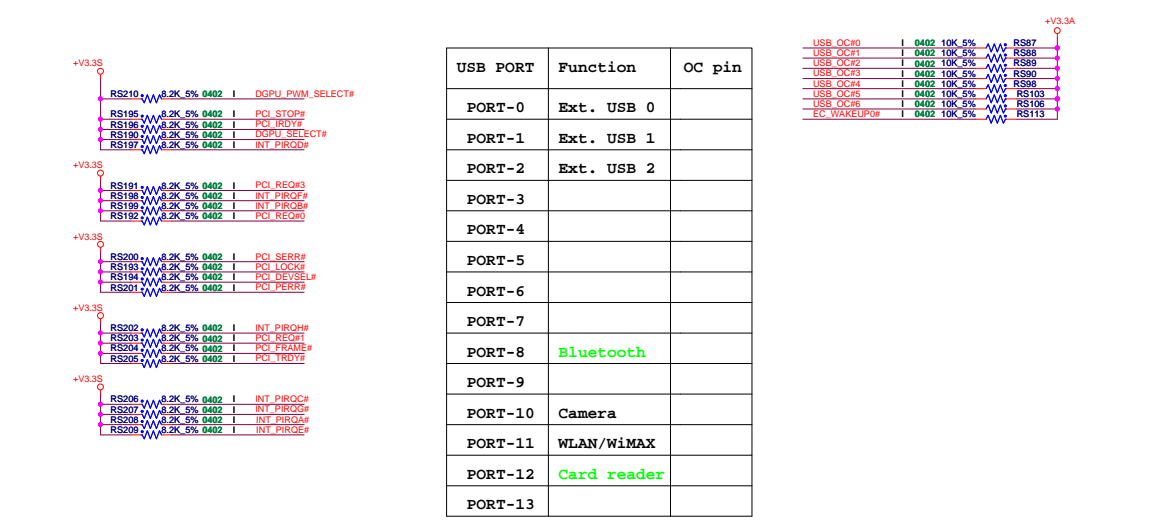
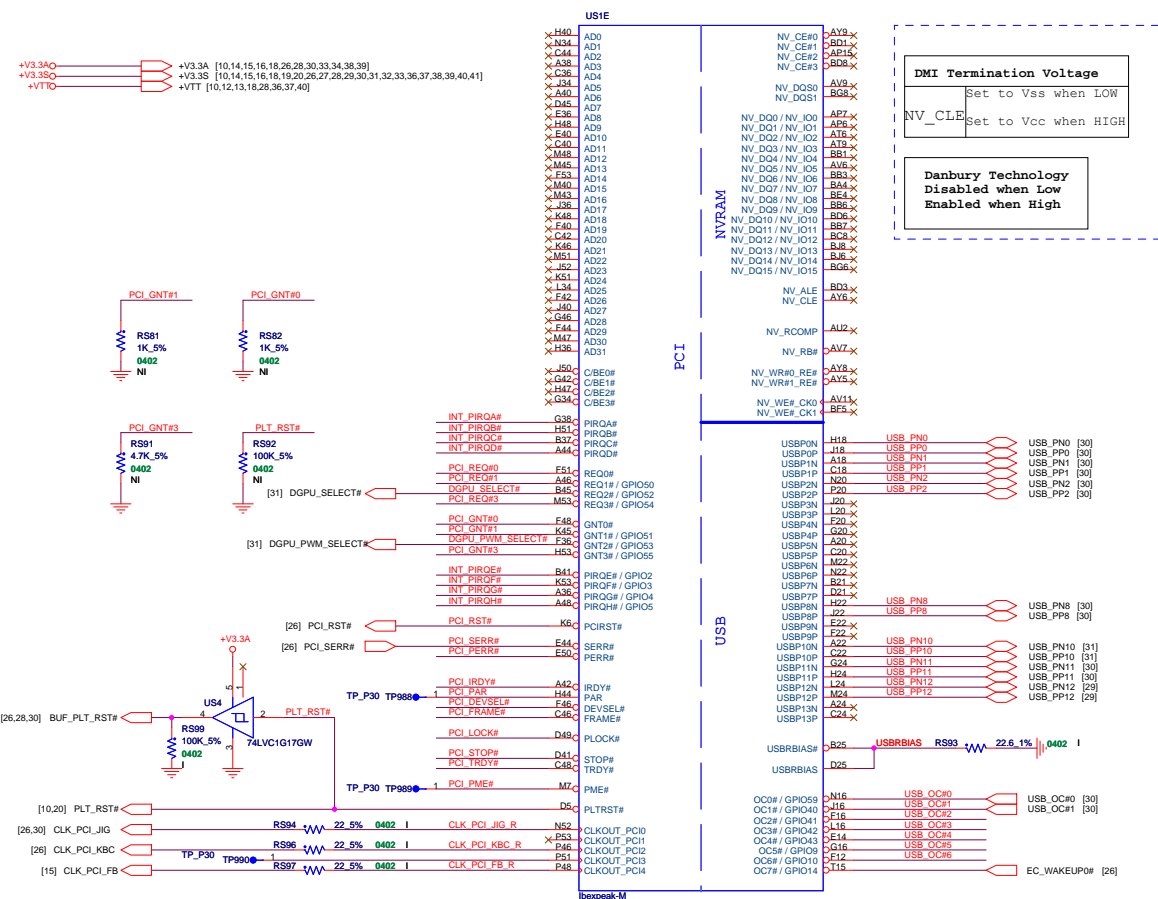




| Port | Function |
|-------|----------|
| Port1 | LAN |
| Port2 | Un-used |
| Port3 | WLAN |
| Port4 | Un-used |
| Port5 | Un-used |
| Port6 | Un-used |
| Port7 | Un-used |
| Port8 | Un-used |

PCI-E Port Table





| USB PORT | Function | OC pin |
|----------|-------------|--------|
| PORT-0 | Ext. USB 0 | |
| PORT-1 | Ext. USB 1 | |
| PORT-2 | Ext. USB 2 | |
| PORT-3 | | |
| PORT-4 | | |
| PORT-5 | | |
| PORT-6 | | |
| PORT-7 | | |
| PORT-8 | Bluetooth | |
| PORT-9 | | |
| PORT-10 | Camera | |
| PORT-11 | WLAN/WiMAX | |
| PORT-12 | Card reader | |
| PORT-13 | | |

DMI Termination Voltage

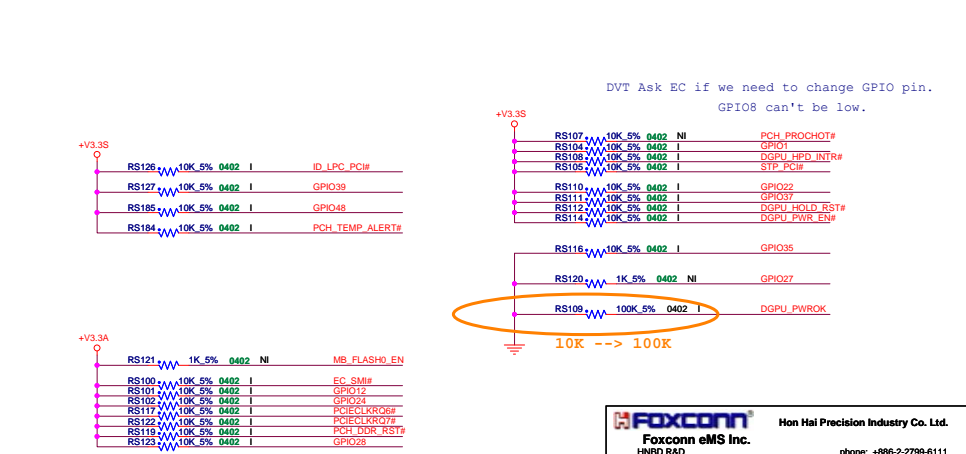
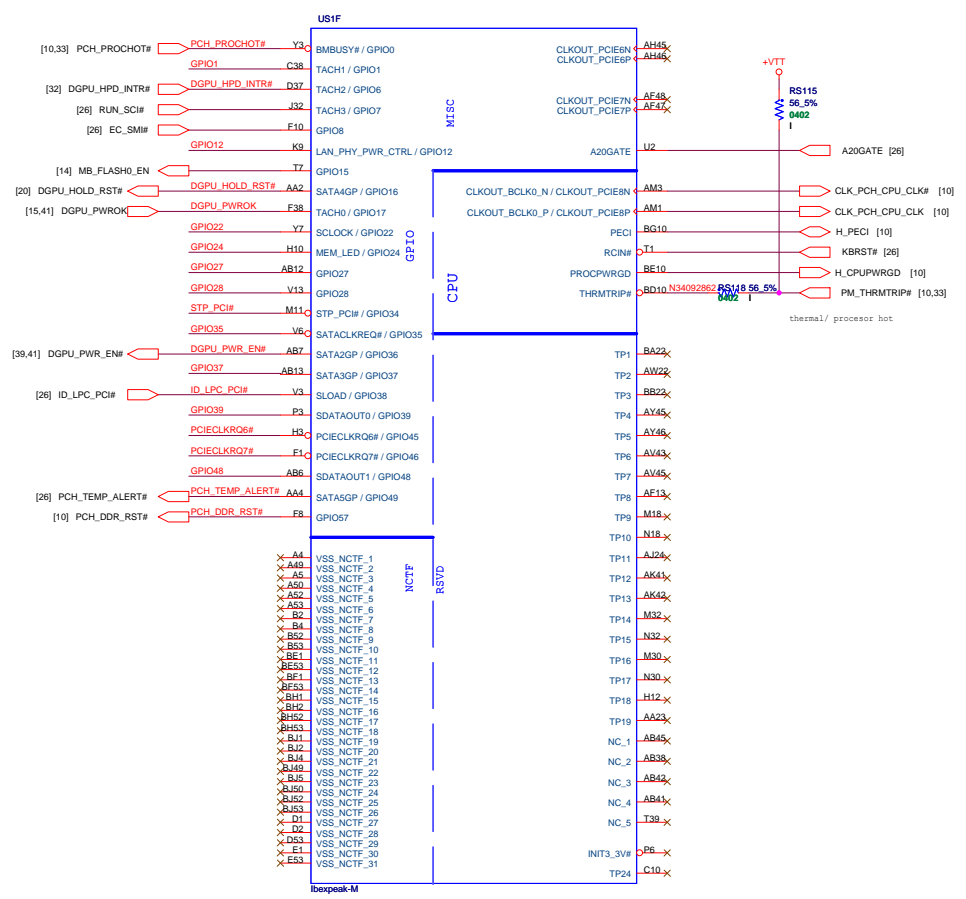
Set to Vss when LOW

Set to Vcc when HIGH

Danbury Technology

Disabled when Low

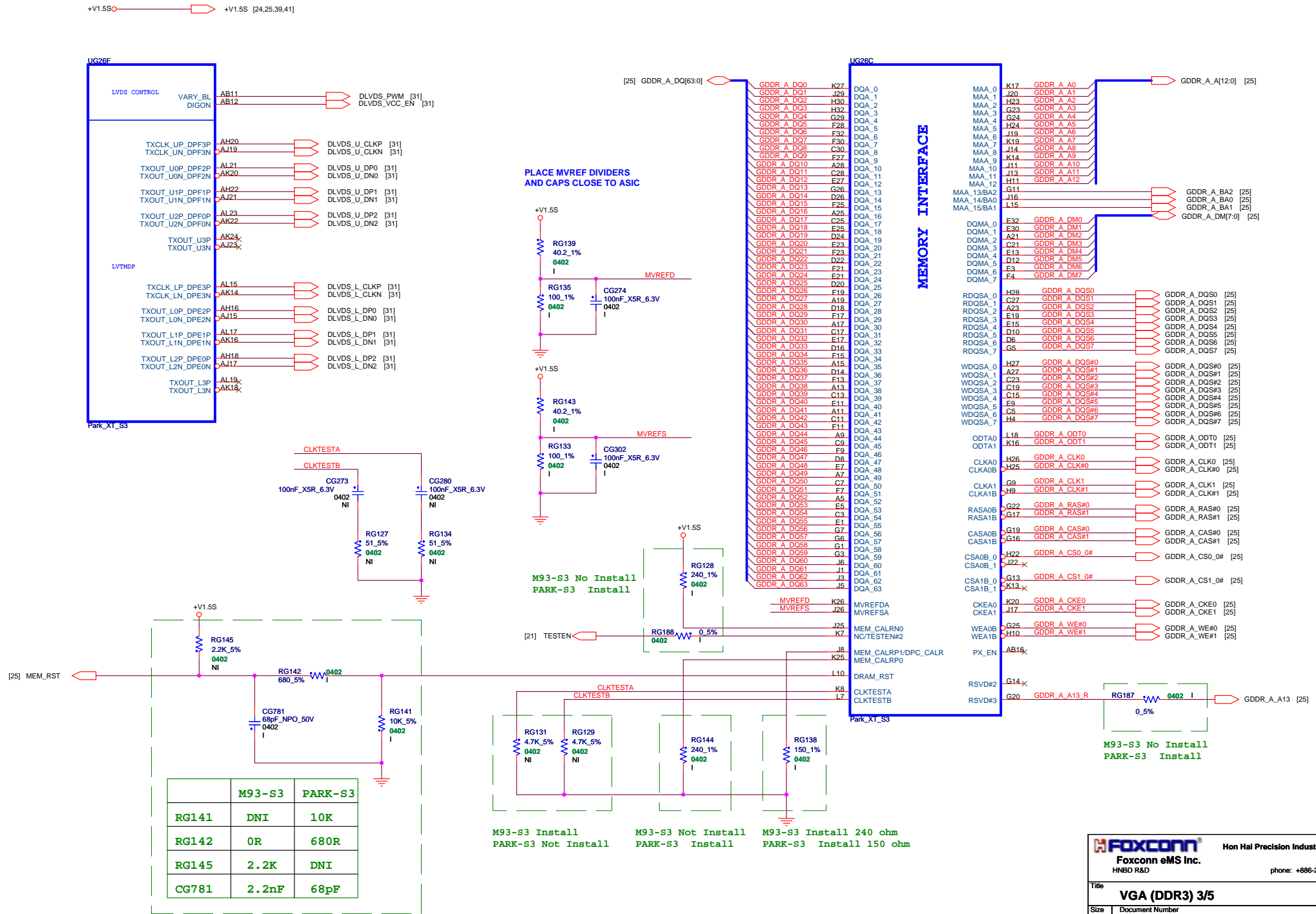
Enabled when High

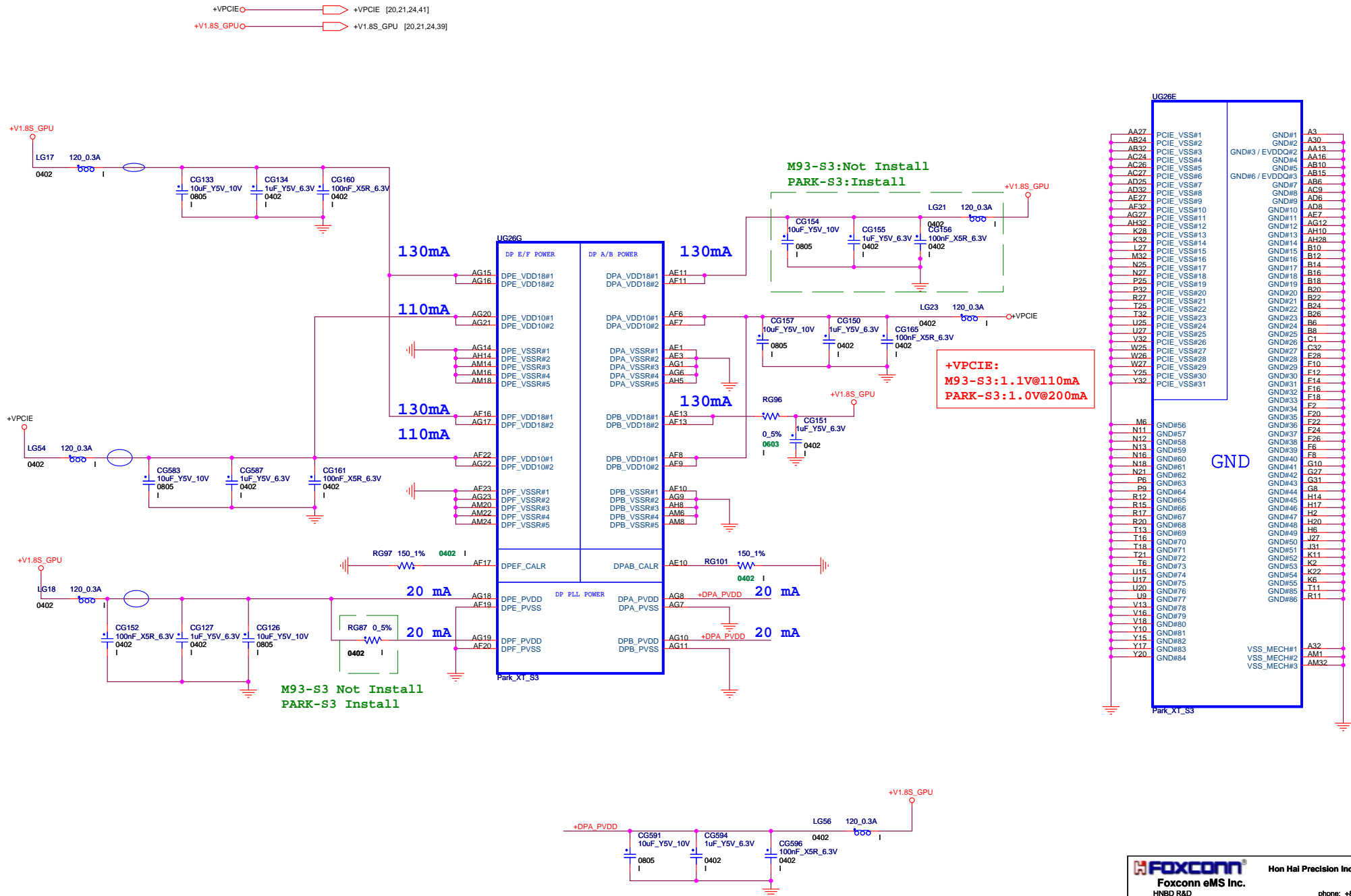


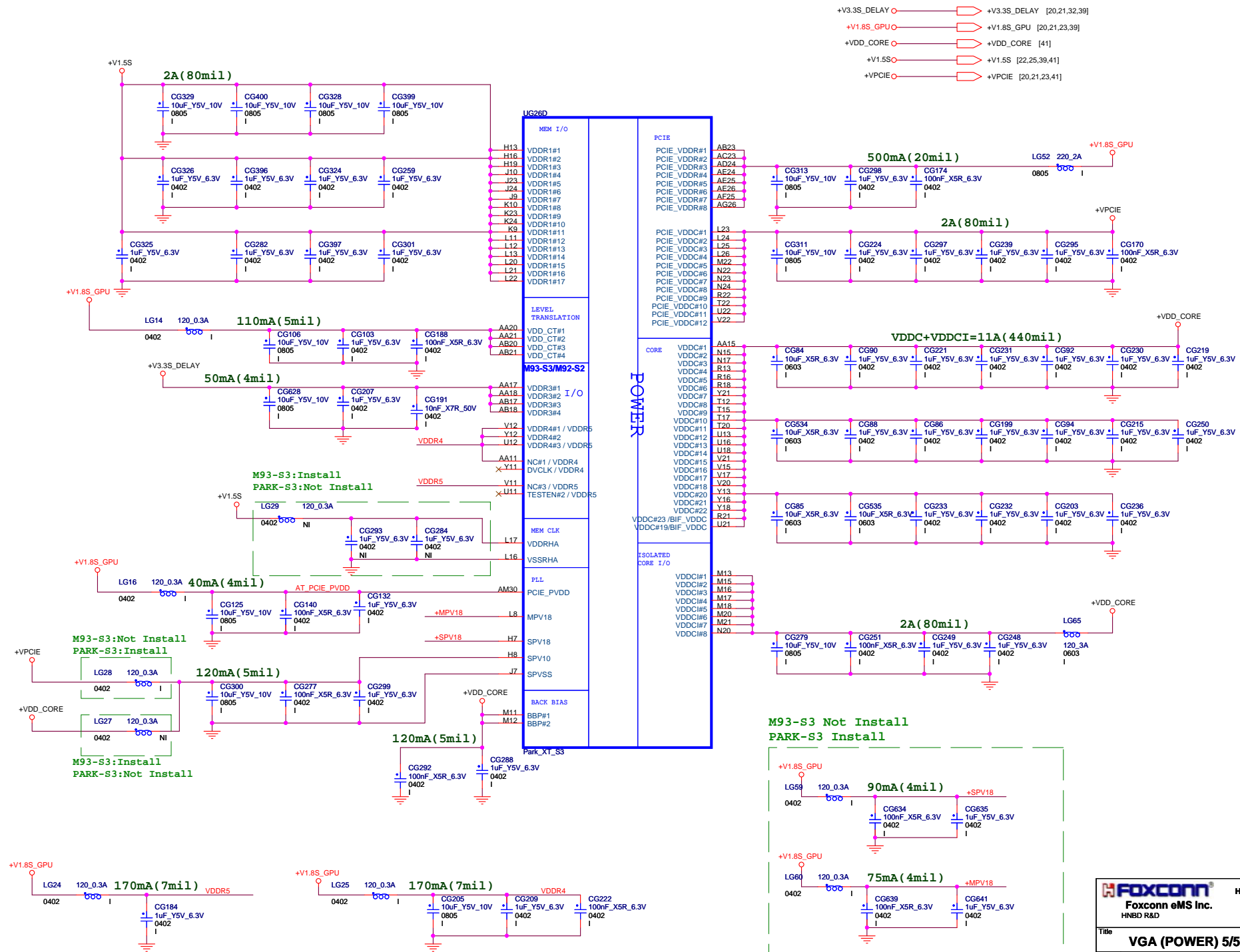






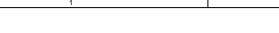
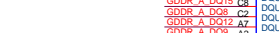
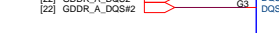
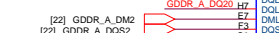
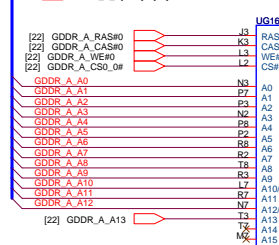






+V1.5S

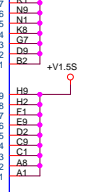
GDDR_A_A[12:0] [22]



+V1.5S

420mA

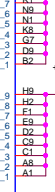
GDDR_A_A[12:0] [22]



+V1.5S

420mA

GDDR_A_A[12:0] [22]



+V1.5S

420mA

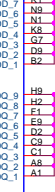
GDDR_A_A[12:0] [22]

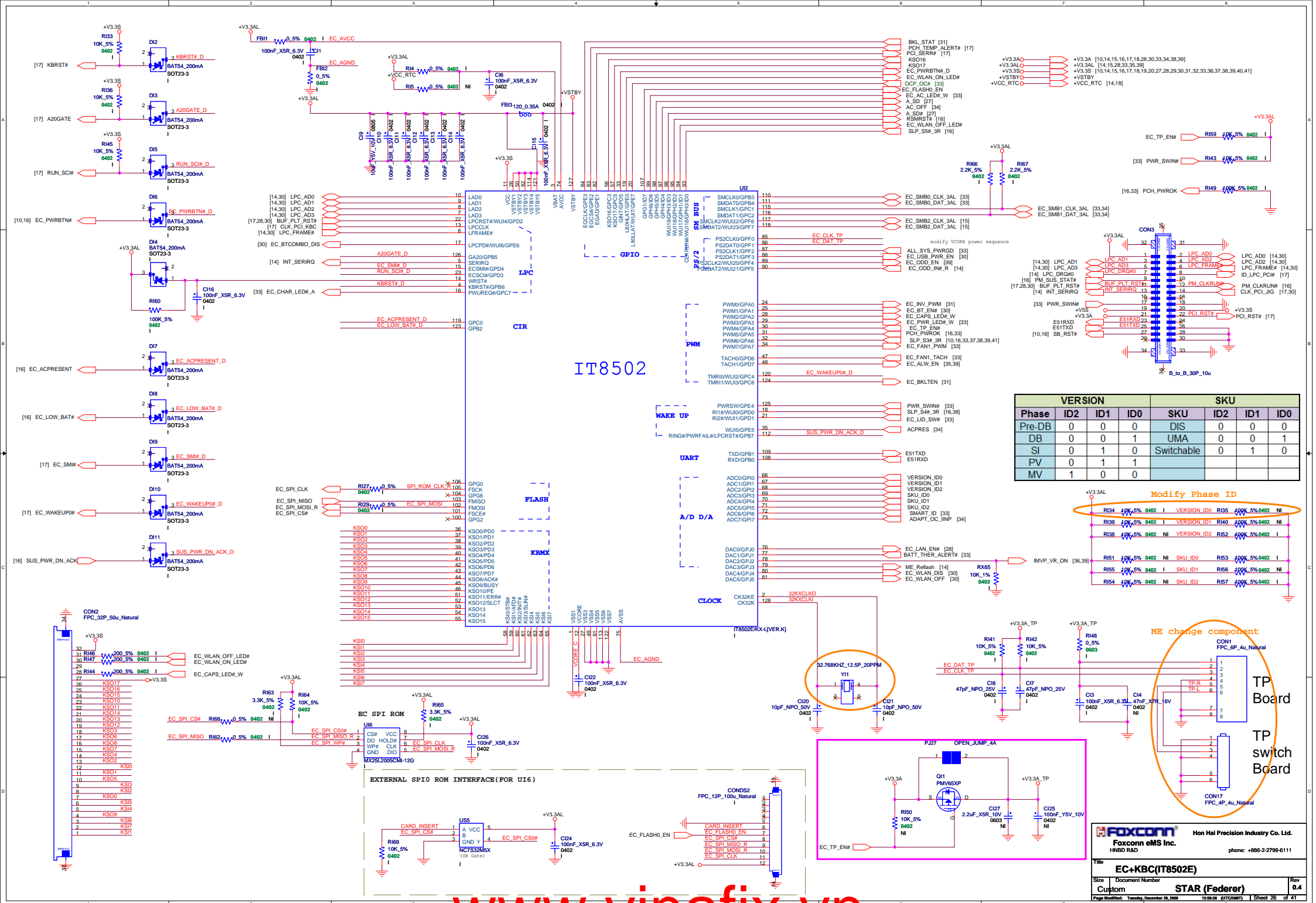


+V1.5S

420mA

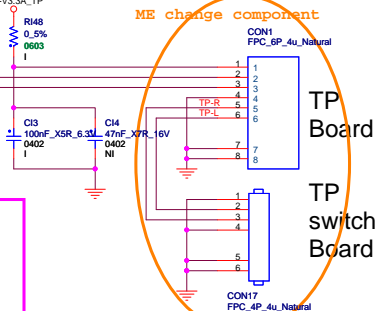
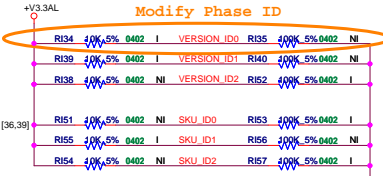
GDDR_A_A[12:0] [22]





IT8502

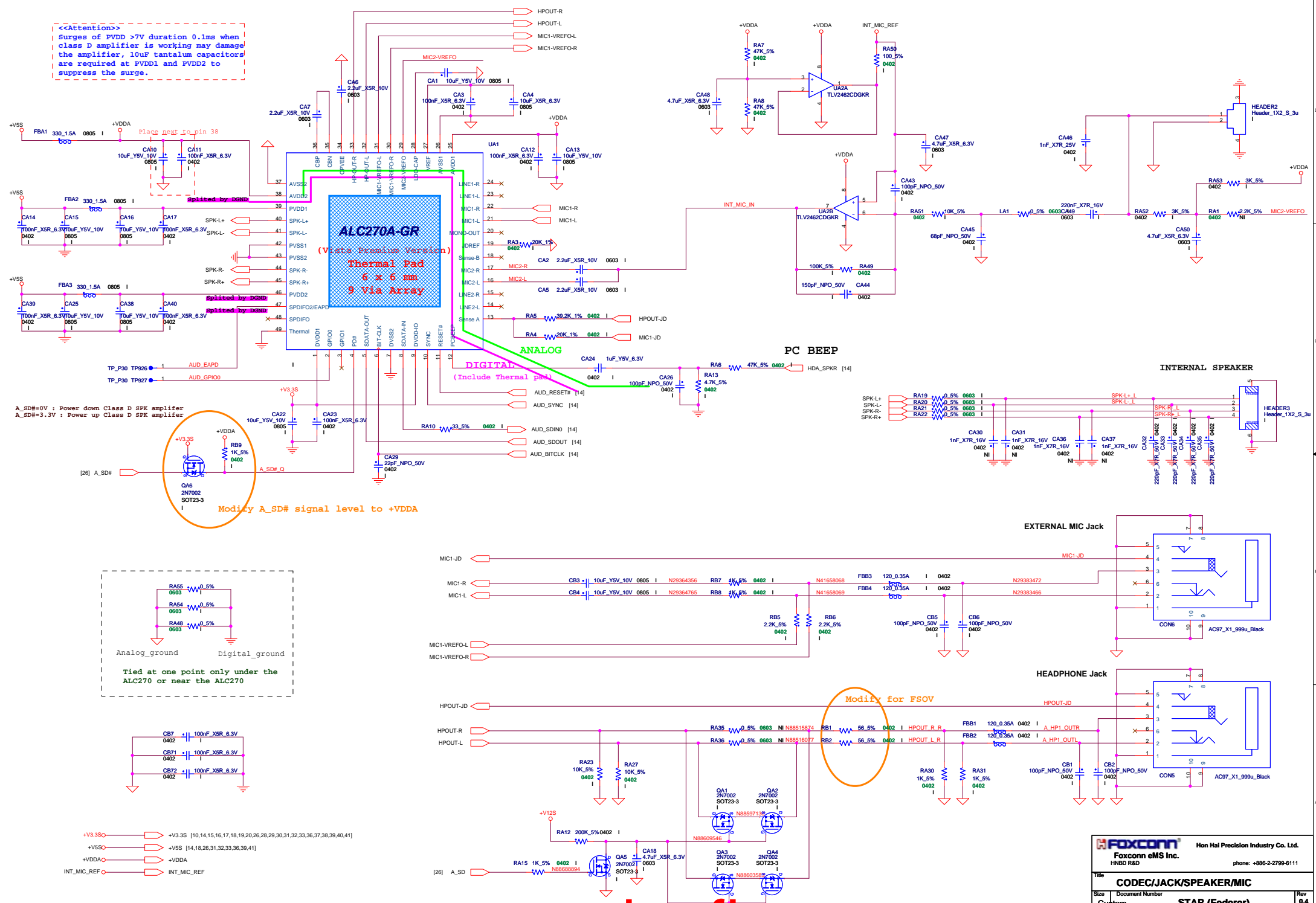
| VERSION | | | | SKU | | | |
|---------|-----|-----|-----|------------|-----|-----|-----|
| Phase | ID2 | ID1 | ID0 | SKU | ID2 | ID1 | ID0 |
| Pre-DB | 0 | 0 | 0 | DIS | 0 | 0 | 0 |
| DB | 0 | 0 | 1 | UMA | 0 | 0 | 1 |
| SI | 0 | 1 | 0 | Switchable | 0 | 1 | 0 |
| PV | 0 | 1 | 1 | | | | |
| MV | 1 | 0 | 0 | | | | |

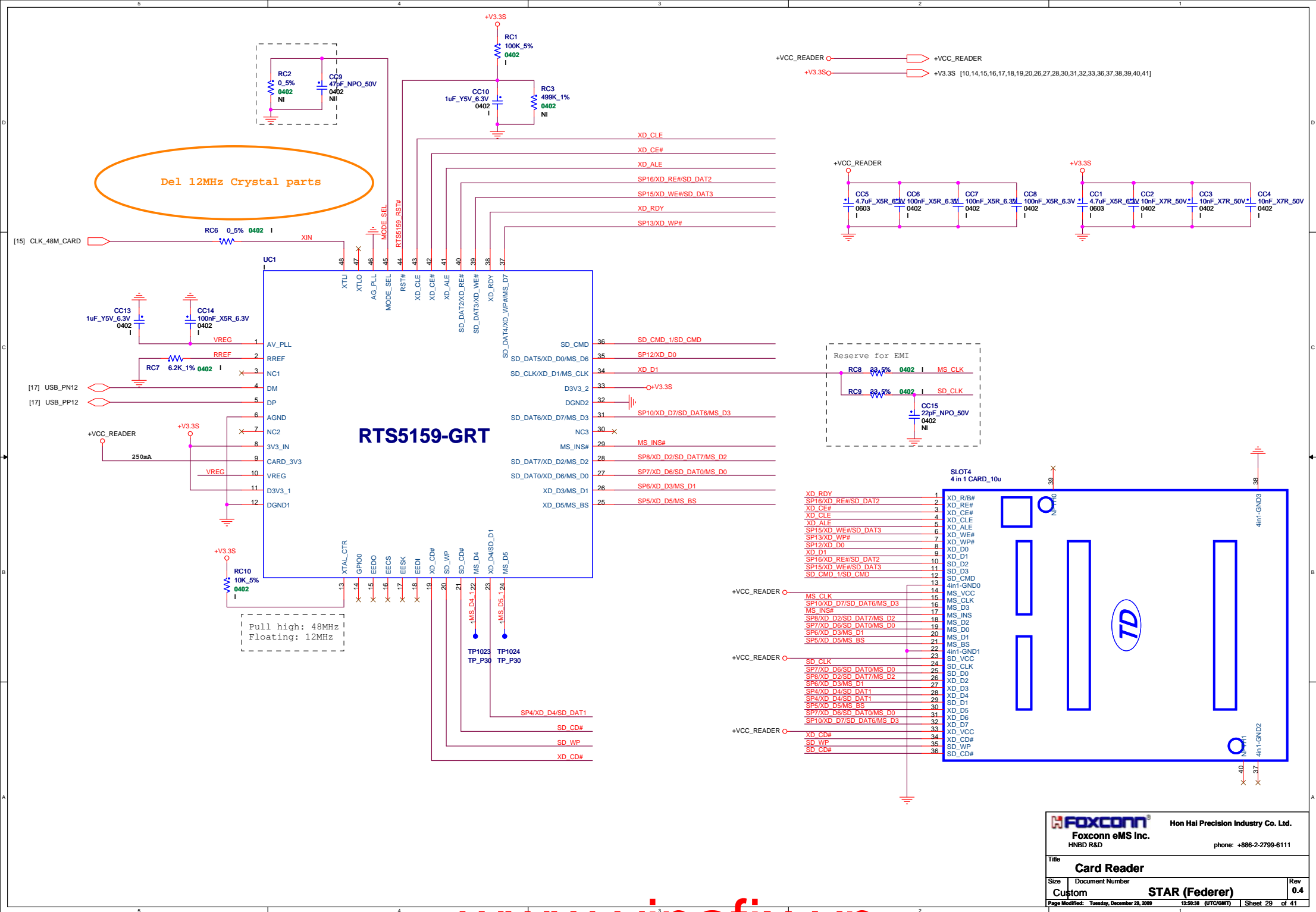


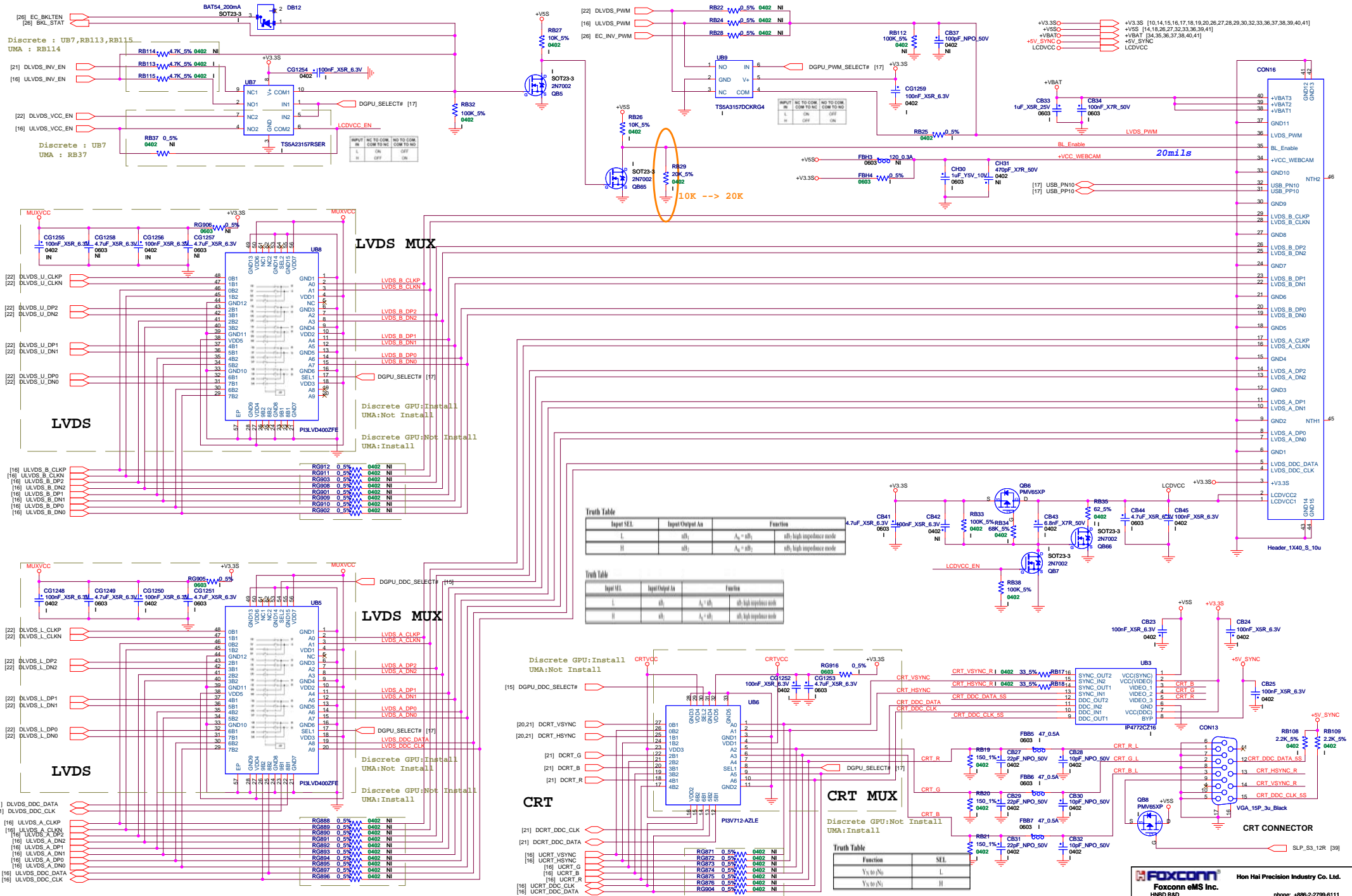
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<<Attention>>
Surges of PVDD >7V duration 0.1ms when class D amplifier is working may damage the amplifier, 10uF tantalum capacitors are required at PVDD1 and PVDD2 to suppress the surge.








| Input SEL | Input/Output An | Function |
|-----------|------------------|---|
| L | all ₁ | A ₁ = all ₁ all high impedance mode |
| H | all ₁ | A ₁ = all ₁ all high impedance mode |

| Input SEL | Input/Output An | Function |
|-----------|------------------|---|
| L | all ₁ | A ₁ = all ₁ all high impedance mode |
| H | all ₁ | A ₁ = all ₁ all high impedance mode |

| Function | SEL |
|----------------------------------|-----|
| Y ₁ to N ₁ | L |
| Y ₁ to N ₁ | H |



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Title

Size

Custom

Document Number

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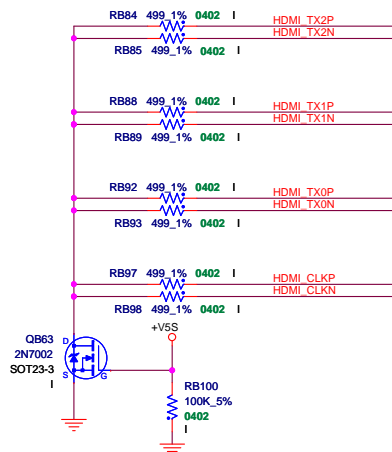
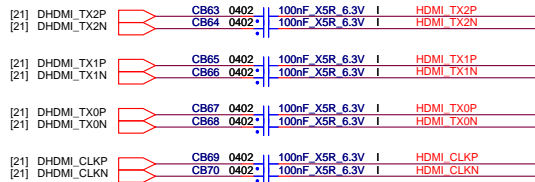
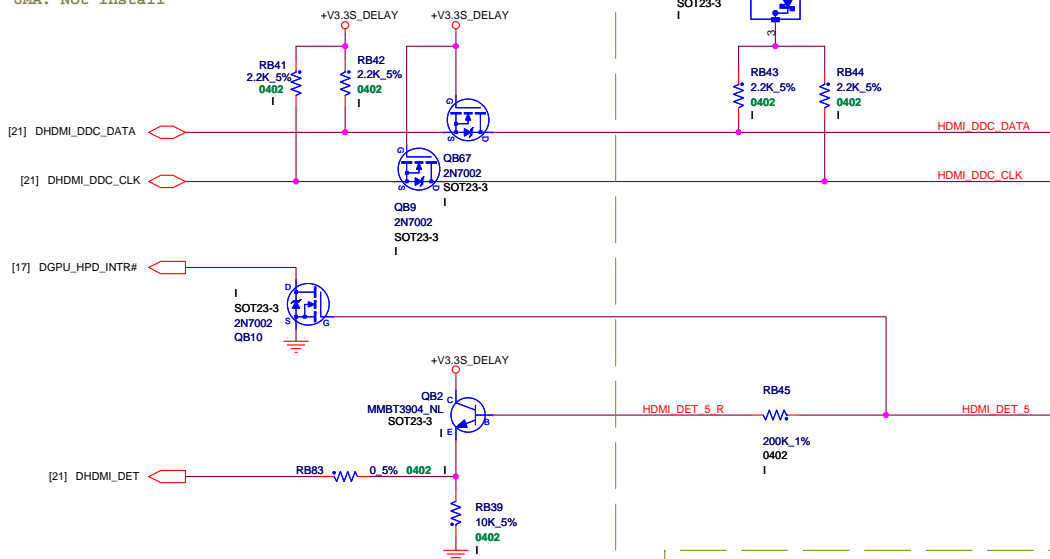
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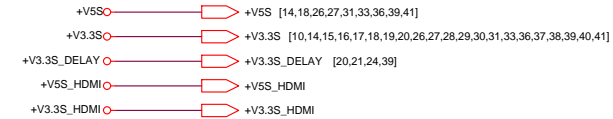
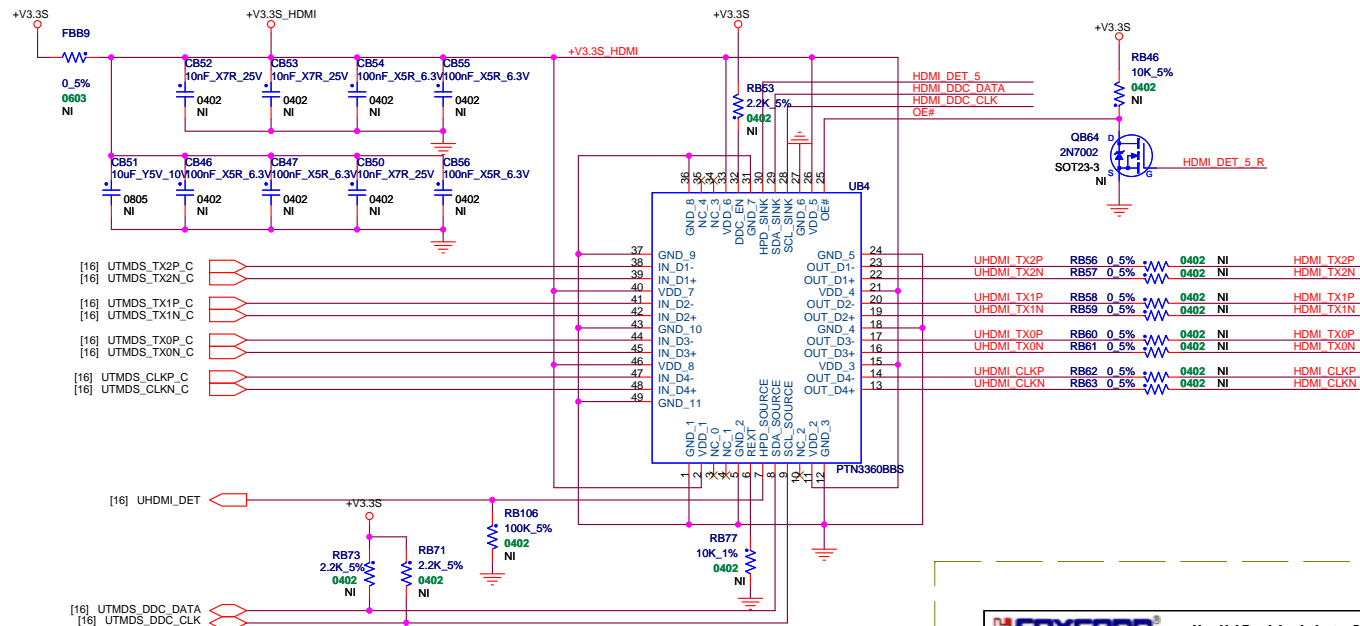
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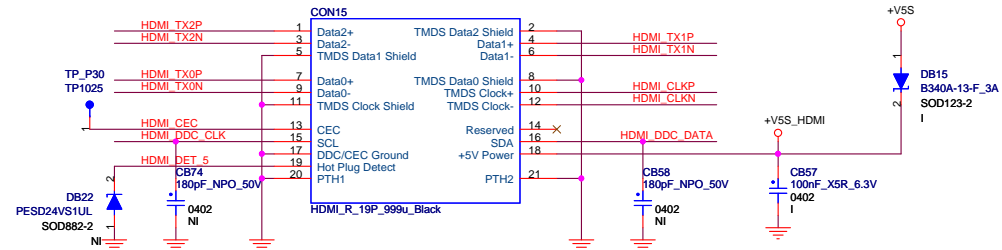
Discrete GPU: Install
UMA: Not Install

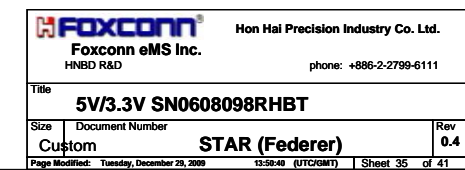


Discrete GPU:Not Install
UMA:Install



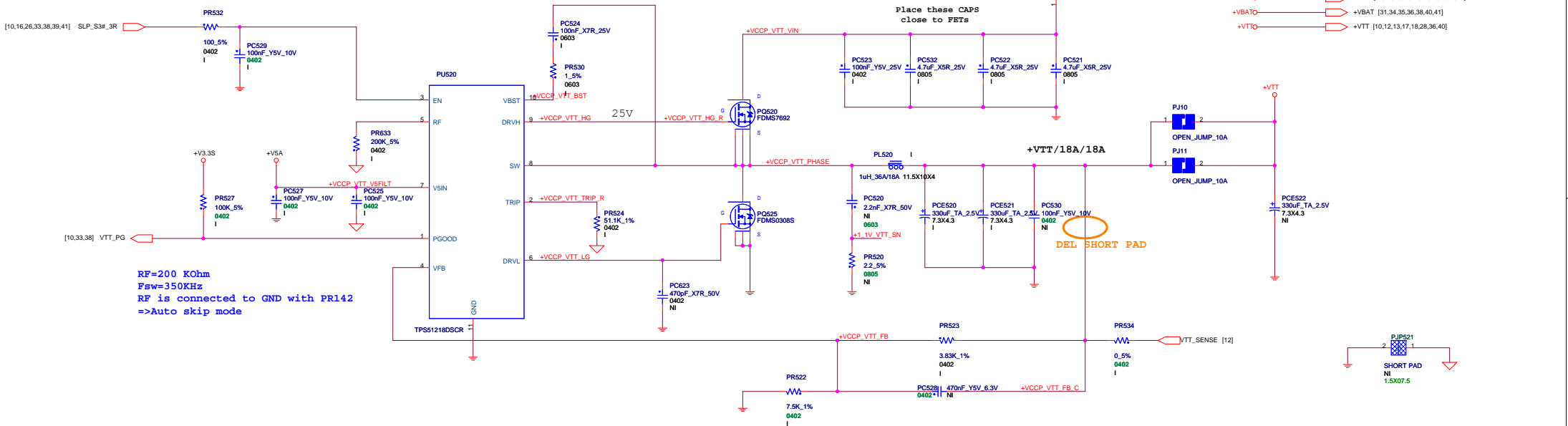
HDMI spec: +5V:4.7V min , 55mA max.



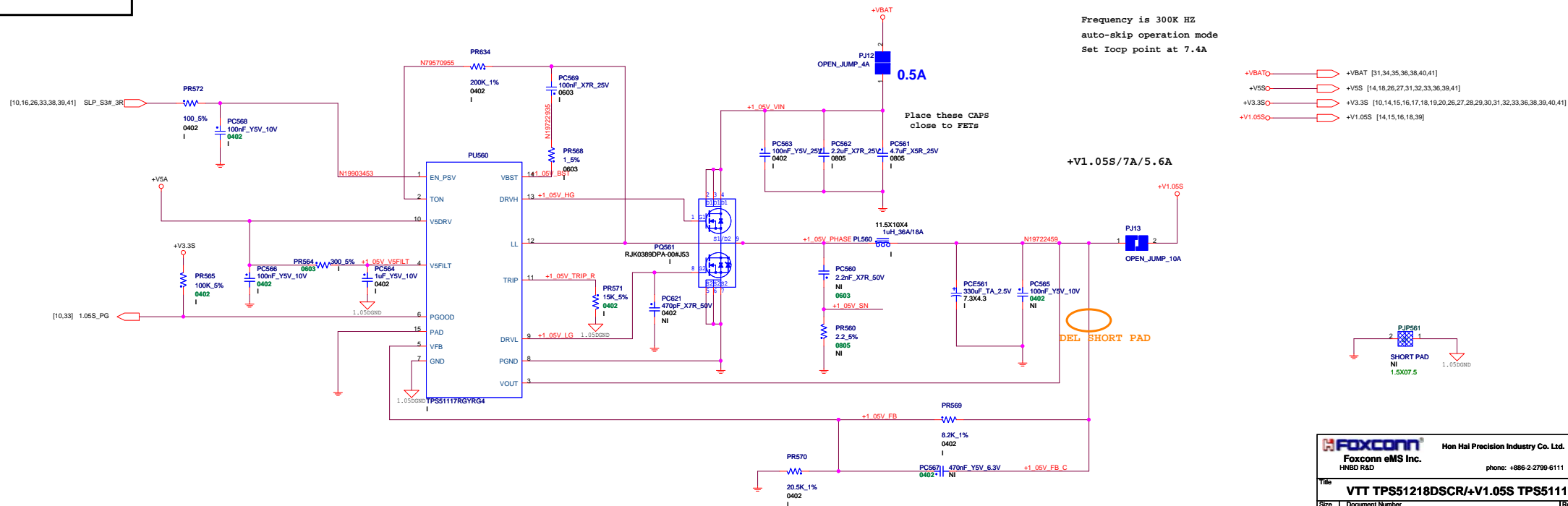


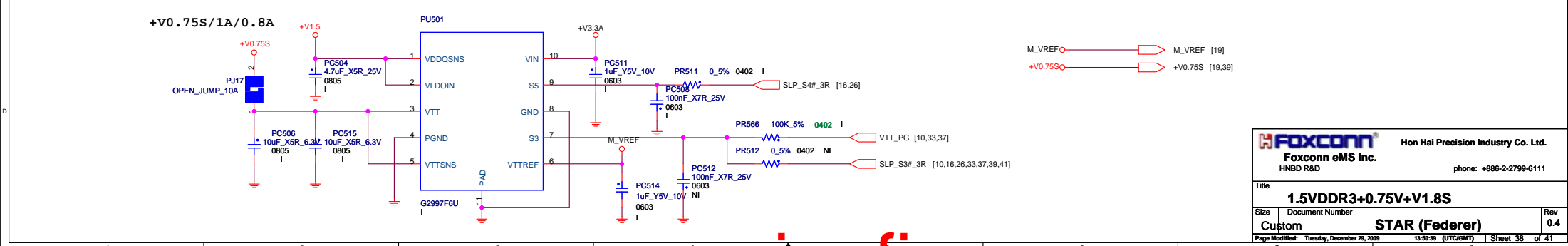
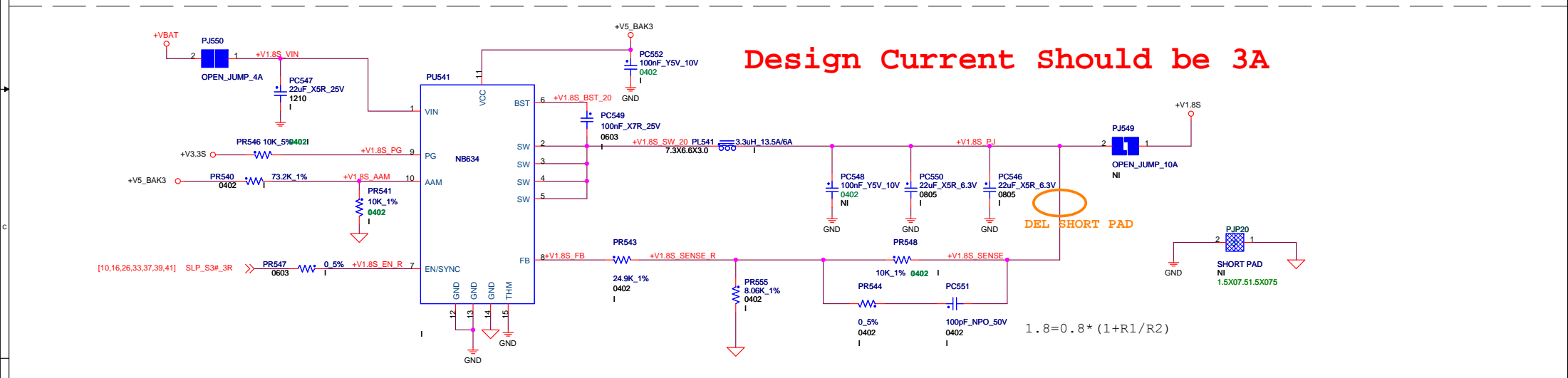
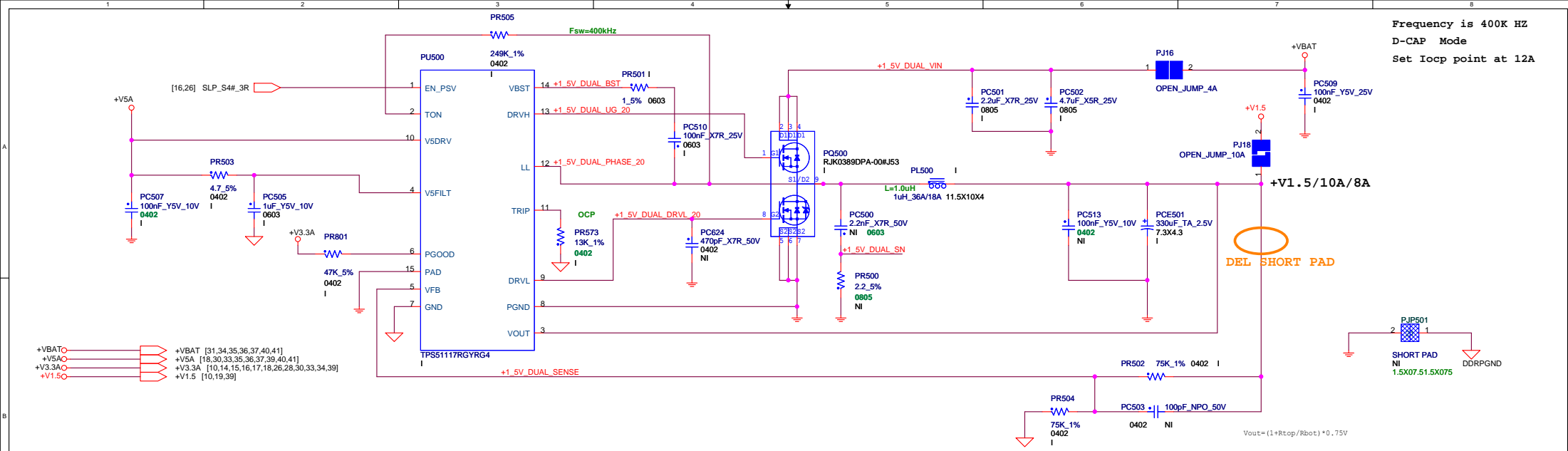


+VTT TPS51218



+V1.05S TPS51117







+VGFXCORE

